An Engineering Validation of the Semi-Classical Trigger Approach for PET Coincidence Finding

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Abstract:
The classical trigger system finds coincidence in time domain by manipulating pulses with accurate arrival time and width. All cables carrying such pulses from front end modules to coincidence module must have well controlled propagation delay and all discriminators generating hit pulses are to be adjusted precisely. Contemporary full digital approaches need only precise timing at the TDC in the front end module and eliminate requirement of accurate timed cables and modules for data merging. However, when the detector hit rate is fluctuated high, some hits may be discarded in the front end without checking for coincidence, which causes not only lower efficiency but also possible inappropriate emphasis or de-emphasis in final image. In the semi-classical trigger PET coincidence approach described in this document, the coarse times of all hits are transmitted to the coincidence module for coincidence check, as in classical trigger system. On the other hand, the communication channels are digital serial links so that no accurately timed cables and merging modules are needed. The advantages of the full digital system, i.e., robustness and confining precise time at the TDC in the front end are preserved. An engineering validation design and test has been done and is discussed in this document.

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Summary:
Coincidence finding architectures in PET or in high energy/nuclear physics experiments are primarily in two flavors: classical trigger type and data-pushing non-trigger type as shown in Fig. 1(a) and (b). In classical trigger systems, all interconnections and merging modules from front-end electronics to the coincidence module must be well-timed. Many contemporary systems employ the non-trigger architectures in which precise time is only needed in the front-end digitization modules. Hit times are digitized and sent via digital serial links to the coincidence/DAQ module in which coincidence is searched. This approach is much more robust and requires no precise timing for the data cable. However, when the hit rate in the front-end fluctuates high, some hits must be discarded to prevent the data link from being jammed. If the hit elimination scheme is not designed appropriately, some statistical feature in the final data may be created artificially. In PET system, some portion of the image can be incorrectly emphasized or de-emphasized.

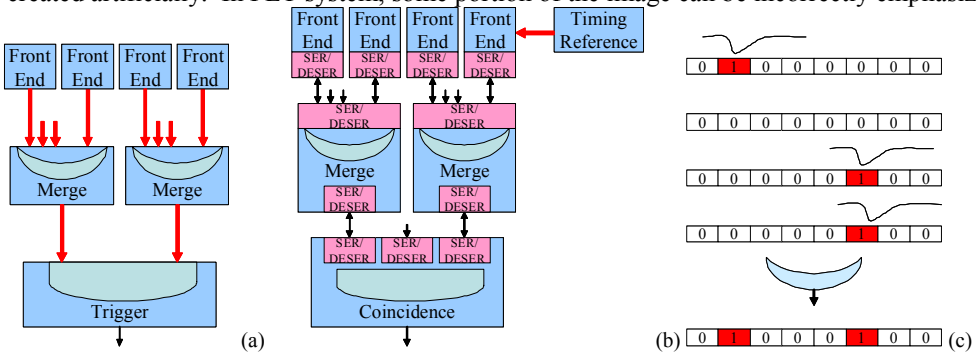

Fig. 1. Coincidence Finding: (a) Classical Trigger System (b) Full Digital Non-trigger System (c) Hit Coding for the Semi-Classical Trigger Approach

The semi-classical trigger approach is a combination of several established schemes with rational selection of options in various aspects. The semi-classical trigger approach uses the same structure as the full digital non-trigger system and maintains the same advantage of robustness with precise timing requirement confined in the front-end digitization modules only. The hits in the front-end module is digitized and stored in a pipeline temporary storage. Instead of sending full digitized data of all hits through the serial link, only one bit is sent out per hit representing the coarse time of the hit. The data sent out is a bit pattern as shown in Fig. 1(c) with each bit representing a short time interval. The link bandwidth to transmit the bit pattern is relatively small and does not vary with the instantaneous hit rate. For example, if each bit represents a 5-ns time interval, a 200 M bits/s (or 250 M bits/s with 8B/10B coding) data link is sufficient to transmit all the hits. No hits are discarded as long as they are in different time intervals. (If in the hits are in the same time interval, they are merged as one hit. This is part of the coincidence algorithm anyway.)

Of course, timing reference distribution is a non-trivial task. We will discuss this in another submission (abstract #1025).

Bit pattern coding described above is not a new idea. However, bit alignment or time interval alignment between different front-end modules needs a simple but careful planning. Unlike it is claimed in some literatures that the serial links for trigger system should have fixed latency, it should be pointed out that the links with fixed latency is NOT required. After power-up and establishment of the link, the timing reference system distributes an initialization command to all the front end modules. All the front-end modules send out a special word as an initialization marker and then the bit patterns of hits. At the receiving end, the bit patterns following the initialization marker are stored in sequence into a temporary FIFO. The bit patterns representing the same hit time at the detector from

different channels may arrive the receiving end at different time, but they are stored in the same address in the FIFO buffers. The coincidence is searched between bit patterns with the same address, regardless their actual arrival time.

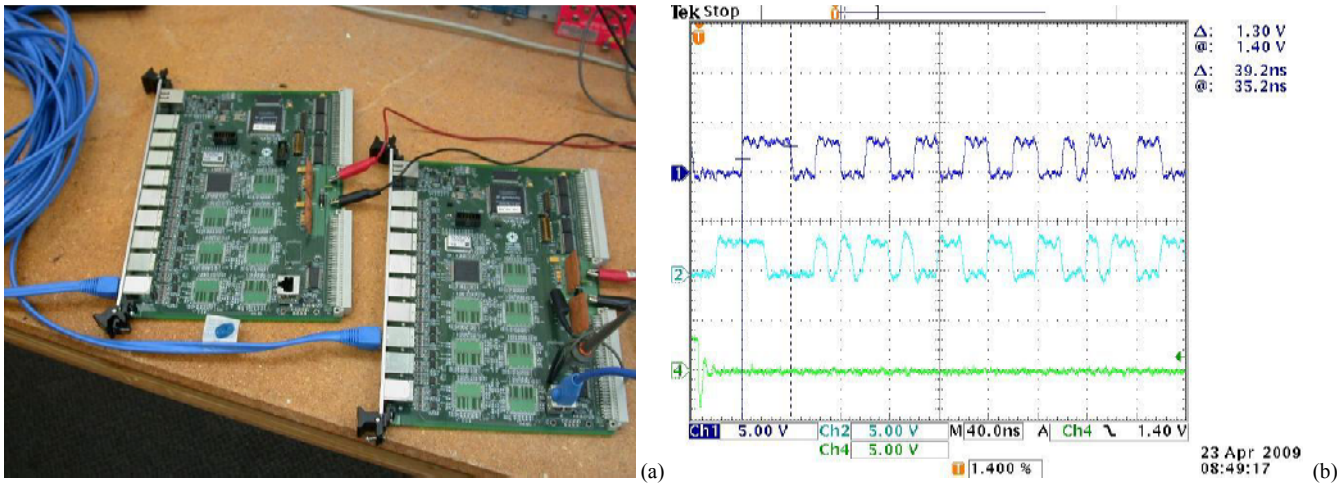

Fig. 2. Engineering Validation Test: (a) Test Modules (b) The FM Serial Link Signals

A simple engineer validation is done with a digital fan-in/fan-out module as shown in Fig. 2(a). (The module was designed for other projects.) The modules are connected together with the RJ-45 connectors via Cat-5 twist pair cables. There are 4 differential LVDS pairs with 100 M bits/s bandwidth each going both input and output directions in each RJ-45 connector. The module on the left is used as a merging module and the one on the right is the coincidence/DAQ module. The FM coding chosen here is for illustrative purpose (but not very efficient) as shown in Fig. 2(b). A bit is coded in a 20 ns time interval with a logic 0 being a non-flipping 20 ns wide pulse and a logic 1 being two 10 ns pulses (i.e., an all-0 sequence is a 25 MHz clock and an all-1 sequence is 50 MHz). The initialization marker is a set of 40 ns wide pulses with the first bit following the last 40 ns pulse immediately. For example, in Fig. 2(b), the channel 1 has a bit pattern 000000000001000 and the channel 2 11010000000100 following the initialization markers. Although the arrival times of the two channels are different, it is very easy to align them inside FPGA.

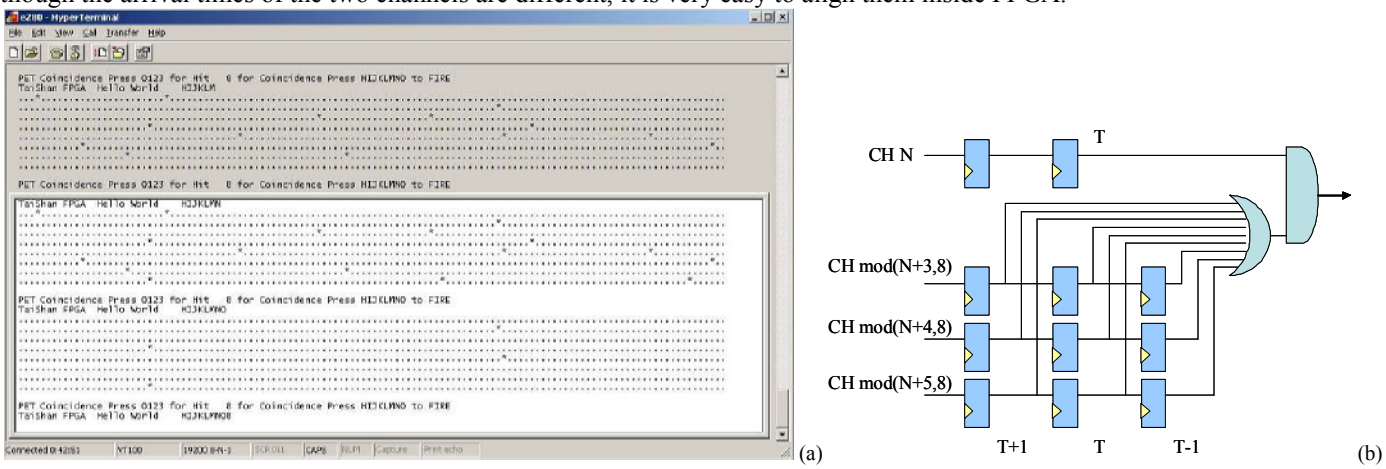

Fig. 3. The Result of Engineering Validation Test: (a) The Screen Dump (b) The Coincidence Logic

Coincidences between 8 input channels are searched in FPGA as illustrated in the screen dump shown in Fig. 3(a) generated by the FPGA via an RS232 serial port. There are 8 lines corresponding to 8 input channels in each section and each character in a line represent a 20 ns time interval, with "*" being logic 1 and "." being logic 0. The top section shows the progress of the FIFO filling. For demo purpose, the arrival time differences are exaggerated so that channels 7 is not filled in the top section. The middle section shows the hits after all inputs arrive. The lower section shows hits that satisfy the coincidence. The coincidence of a hit in channel N and time bin T is searched in channels: mod(N+3,8), mod(N+4,8) and mod(N+5,8) for time bins: T-1, T and T+1, a total of 9 logic terms as shown in Fig. 3(b).

The valid coincidence becomes a trigger command that is sent using serial link via the RJ-45 connector back to the front-end digitizer so that hit data in the trigger time interval can be readout. Clearly the required bandwidth of triggered data is significantly smaller than that of raw data. The bit pattern of hits, trigger command and triggered data are all carried in a single Cat-5 cable and no separate interconnections are needed. The simplicity of the interconnection between modules is a key feature that ensures reliability of the final system. In our full paper, a detailed scheme and a set of options of utilizing the four differential pairs in the Cat-5 cable with RJ-45 connectors will be discussed.

With the semi-classical trigger approach, it is possible to build the coincidence system at relatively low cost. It can be seen that a merging module shown in Fig. 2(a) serves 8 front-end boards. If we assume a front-end board handles 16 PMTs, then 8 merging modules plus a coincidence/DAQ module can serve up 64 front-end boards or a camera with 1024 PMTs.